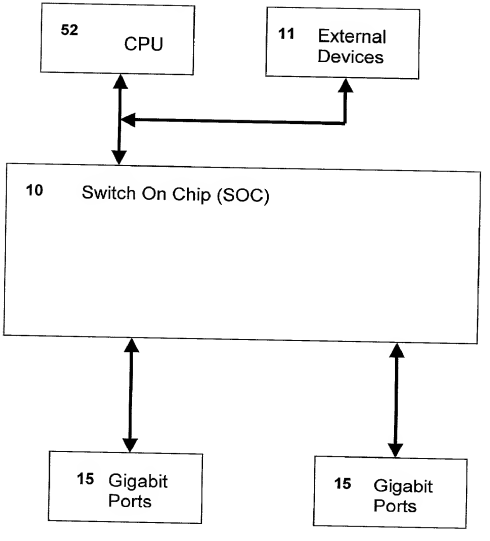
52 CPU
11 External Devices
10 Switch On Chip (SOC)
15 Gigabit Ports
15 Gigabit Ports

Fig. 1

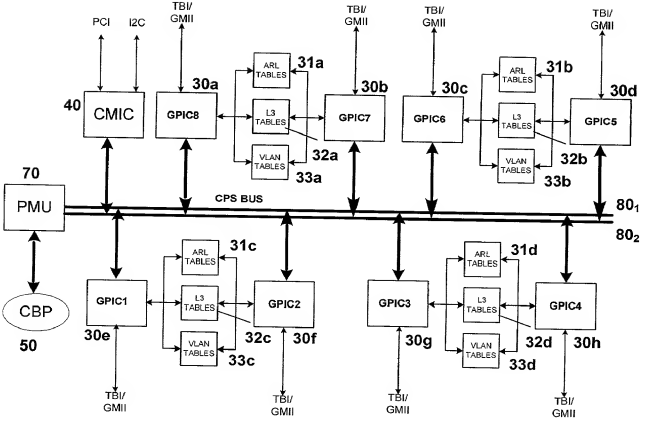
PCI
I2C
TBI/ GMII
CMIC
40
GPIC8
30a
ARL TABLES
L3 TABLES
VLAN TABLES
31a
32a
33a
GPIC7
30b
GPIC6
30c
31b
32b
33b
GPIC5
30d
70
PMU
CPS BUS
80₁
80₂
CBP
50
GPIC1
30e
31c
32c
33c
GPIC2
30f
GPIC3
30g
31d
32d
33d
GPIC4
30h

Fig. 2

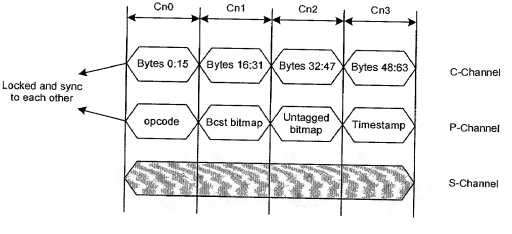
Cn0
Cn1
Cn2
Cn3
Locked and sync to each other
Bytes 0:15
Bytes 16:31
Bytes 32:47
Bytes 48:63
C-Channel
opcode
Bcst bitmap
Untagged bitmap
Timestamp
P-Channel
S-Channel

Fig. 3

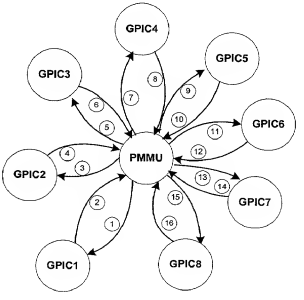

Fig. 4

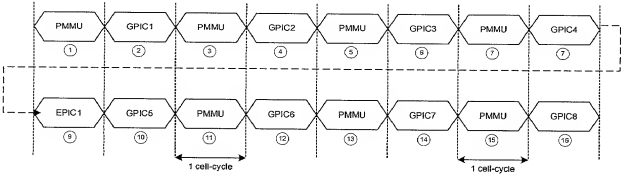

Fig. 5

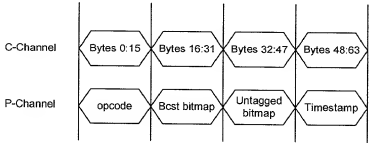

Fig. 6

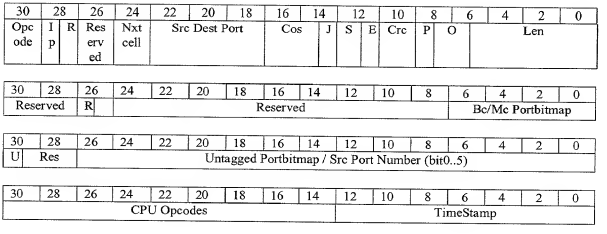
30 28 26 24 22 20 18 16 14 12 10 8 6 4 2 0
Opc ode
I p
R
Res erv ed
Nxt cell
Src Dest Port
Cos
J
S
E
Crc
P
O
Len
Reserved
R
Reserved
Bc/Mc Portbitmap
U
Res
Untagged Portbitmap / Src Port Number (bit0..5)
CPU Opcodes
TimeStamp

Fig. 7

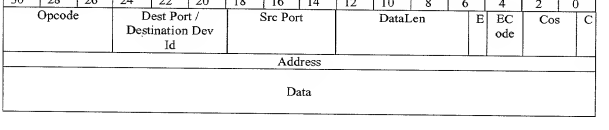
30 28 26 24 22 20 18 16 14 12 10 8 6 4 2 0
Opcode
Dest Port / Destination Dev Id
Src Port
DataLen
E
EC ode
Cos
C
Address
Data

Fig. 8

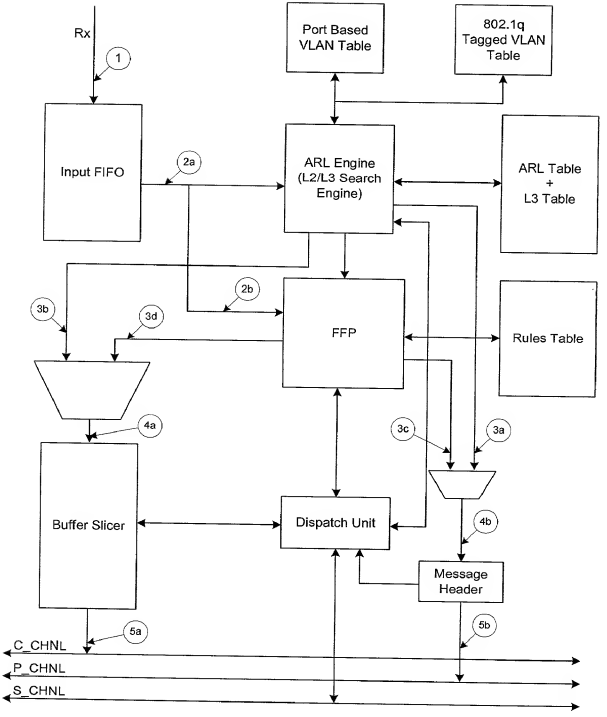
Rx
1
Port Based VLAN Table
802.1q Tagged VLAN Table
Input FIFO
2a
ARL Engine (L2/L3 Search Engine)
ARL Table + L3 Table
2b
3b
3d
FFP
Rules Table
4a
3c
3a
Buffer Slicer
Dispatch Unit
4b
Message Header
5a
5b
C_CHNL
P_CHNL
S_CHNL

Fig. 9